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10/581,263	04/16/2007	Samuel J. Anderson	GWS-004	2322

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EXAMINER	
AHMED, SELIM U	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
09/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/581,263	ANDERSON, SAMUEL J.	
	Examiner	Art Unit	
	SELIM AHMED	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial office action based on the application filed on 04/06/2007. Claims 1-25 with preliminary amendment and 26-31 as newly added claims are considered here.
2. The Preliminary Amendment filed on 06/1/2006 has been entered.

Priority

3. Acknowledgment is made of applicant's priority under PCT/US2004/40197 filed on 12/1/2004 and provisional application 60/526,926 filed on 12/3/2003.

Information Disclosure Statement

4. No IDS has been filed under this application.

Oath/Declaration

5. The oath or declaration filed on 4/16/2007 is acceptable.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, claim elements such as analog circuit structure (claims 22-25), a plurality of semiconductor chips within package (claim 26), a plurality of the pairs of lateral power transistor

devices (claims 27, 30) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

a. Antecedent basis of analog integrated circuit as outlined in claims 22-26.

b. Antecedent basis of a plurality of the pairs of lateral power transistors as outlined in claim 30.

c. Antecedent basis for semiconductor package comprises a plurality of the semiconductor chips as outlined in claim 26.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-8, 11-19, 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemtsev et al (US 2004/0245638; Nemtsev hereinafter)

With regard to claim 1, Nemtsev discloses a semiconductor device package e.g. Fig.6, comprising: semiconductor chip 10 comprising a lateral power transistor device (para[0001, 0002]) formed therein, said semiconductor chip 10 having an upper surface (Fig. 5, upper connection surface of 10), and a terminal 500 disposed on said upper surface said terminal having a conductive bump 500 selected from the group consisting of a ball bump 500 and a pillar bump disposed thereon; a metal lead frame 920 spanning said upper surface of said semiconductor Chip, said metal lead frame being in electrical contact

(para[0025]) with said conductive bump; and a capsule 910 encasing said semiconductor chip and at least a portion of said metal lead frame.

With regard to claim 2, e.g. Figs. 4-6, elements 401, 500, 501 of Nemtsev discloses the semiconductor package as in claim 1 wherein-the terminal is selected from the group consisting of a source terminal, a drain terminal, and a gate terminals.

With regard to claim 3, para[0048] of Nemstev discloses the semiconductor package as in claim 1 wherein opposite ends of said metal lead frame protrude from opposite sides of said capsule.

With regard to claim 4, para[0025] of Nemstev discloses the semiconductor package as in claim 1 wherein said pillar bump comprises copper and a conductive solder.

With regard to claim 5, para[0025] of Nemstev discloses the semiconductor package as in claim 1 wherein said conductive ball comprises a conductive solder.

With regard to claim 6, para[0002] of Nemstev discloses the semiconductor package as in claim 1 wherein said lateral power transistor device

comprises a lateral power metal oxide field effect transistor.

With regard to claim 7, para[0048] of Nemstev discloses the semiconductor package as in claim 1 wherein said lead frame comprises a conductive metal (plated Cu).

With regard to claim 8, para[0048] of Nemstev discloses the semiconductor package as in claim 7 wherein said conductive metal comprises copper (plated Cu).

With regard to claim 11, para[0025] of Nemstev discloses the semiconductor package as in claim 1 wherein said electrical contact is formed by conductive solder comprising at least one of tin and epoxy.

With regard to claim 27, e.g. Fig. 1 of Nemstev discloses the semiconductor package as in claim 1, wherein the semiconductor chip comprises a plurality of the lateral power transistor devices formed therein.

With regard to claim 28, e.g. Figs. 4& 6 of Nemstev discloses the semiconductor package as in claim 1, wherein the lateral power transistor comprises a plurality of terminals 500 (101), 500 (201), 401 disposed on said upper surface, the plurality of terminals comprising a source terminal 500 (101), a

drain terminal 500(201), and a gate terminal 401, each of said source, drain, and gate terminals having a conductive bump 500 selected from the group consisting of a ball 500 bump and a pillar bump disposed thereon.

With regard to claim 12, Nemtsev discloses a semiconductor device package e.g. Figs. 6, 1 comprising: monolithic semiconductor structure e.g. Fig. 1 comprising a pair of lateral power transistor devices e.g. Fig. 1 formed combined on a single semiconductor substrate 12; said semiconductor structure having an upper surface (e.g. Fig. 6, upper connection surface of 10) and terminals 500 disposed on said upper surface thereof; each said terminal having a conductive bump 500 selected from the group consisting of a ball bump 500 and a pillar bump disposed thereon; a metal lead frame 920 spanning said upper surface of said semiconductor structure, said metal lead frame being in electrical contact (para[0025]) with said conductive bump; and a capsule 920 encasing said semiconductor structure and at least a portion of said metal lead frame (Fig. 6).

With regard to claim 13, e.g. Figs. 4-6, elements 401, 500, 501 of Nemtsev discloses the semiconductor package as in claim 12 wherein the terminal is selected from the group consisting of a source terminal, a drain terminal, and a gate terminals.

With regard to claim 14, para[0048] of Nemstev discloses the semiconductor package as in claim 12 wherein opposite ends of said metal lead frame protrude from opposite sides of said capsule.

With regard to claim 15, para[0025] of Nemstev discloses the semiconductor package as in claim 12 wherein said pillar bump comprises copper and a conductive solder.

With regard to claim 16, para[0025] of Nemstev discloses the semiconductor package as in claim 12 wherein said conductive ball comprises a conductive solder.

With regard to claim 17, para[0002] of Nemstev discloses the semiconductor package as in claim 1 wherein said lateral power transistor device comprises a lateral power metal oxide field effect transistor.

With regard to claim 18, para[0048] of Nemstev discloses the semiconductor package as in claim 12 wherein said lead frame comprises a conductive metal (plated Cu).

With regard to claim 19, para[0048] of Nemstev discloses the semiconductor package as in claim 18 wherein said conductive metal comprises copper (plated

Cu).

With regard to claim 29, e.g. Fig. 1 of Nemstev discloses the semiconductor package as in claim 12, wherein the semiconductor package comprises a plurality of the monolithic semiconductor structure.

With regard to claim 30, e.g. Figs. 3 & 4 of Nemstev discloses the semiconductor package as in claim 12, wherein the monolithic semiconductor structure comprises a plurality of the pairs of lateral power transistors devices formed on a single semiconductor substrate.

With regard to claim 31, e.g. Figs. 4 &6 of Nemstev discloses semiconductor package as in claim 12, wherein each of the lateral power transistor devices comprises a plurality of terminals 500 (101), 500(201), 401 disposed on said upper surface, the plurality of terminals comprising a source 500(101) terminal, a drain 500(201) terminal, and a gate terminal 401, each of said source, drain, and gate terminals having a conductive bump 500 selected from the group consisting of a ball bump 500 and a pillar bump disposed thereon.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 9-10, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemstev et al (US 2004/0245638) as applied to claims 1 or 12 and further in view of Tuttle (US 6559521).

With regard to claims 9-10, or 20-21 Nemtsev discloses the limitations of claim 1 or 12 with the exception of the semiconductor package wherein said capsule comprises a non-conductive molding compound or said capsule comprises a plastic respectively. However, in col. 5, lines 26-39 of Tuttle discloses the capsule i.e. molds compound comprises a non-conductive particle or a plastic compound. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Nemtsev's mold compound with Tuttle's mold compound for predictable result of isolating leads from being shorted.

10. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemstev (US 2004/0245638) as applied to claim1 or 12 and further in view of Eden et al (US 2004/0135168; Eden hereinafter).

With regard to claims 22-25, Nemtsev discloses the limitations of claim 1 or 12 with the exception of the semiconductor package wherein said lateral power transistor device comprises an analog integrated circuit or an integrated MOSFET and analog circuit structure. However, in Fig. 4, element 60 of Eden discloses of the semiconductor package wherein said lateral power transistor device comprises an analog integrated circuit or an integrated MOSFET and analog circuit structure. It would have been obvious to one having ordinary skill in the art at the time of the invention to include an analog integrated circuit with the integrated power MOSFET for improving power conversion operations or other operations requiring controlled switching of the power semiconductor device.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nemstev (US 2004/0245638) as applied to claim1 and further in view of Knapp et al (US 2003/0201520; Knapp hereinafter).

With regard to claims 26, Nemtsev discloses the limitations of claim 1 with the exception of the semiconductor package wherein the semiconductor package comprises a plurality of the semiconductor chips. However, in Fig. 2 of Knapp discloses a semiconductor package 21 comprises a plurality of the semiconductor chips 70, 130. It would have been obvious to one having ordinary skill in the art at the time of the invention to include a plurality of chips within a semiconductor package for greater functionality.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA
09/08

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